Specification Amendments

Please replace paragraph 003 with the following re-written paragraph:

003 Contact interconnects, also referred to as vias, are particularly critical for making contact with active areas of a transistor device including active contact regions such as the gate electrode and source and drain (S/D) regions. For example, as characteristic dimensions of transistor devices are scaled down to deep submicron dimensions, the contact opening width allowable is increasing limited due to the shrinking size of the contact areas. Conventional processing steps such as photolithography and reactive ion etching have increasingly limited process windows in order to make reliable contacts ~~while~~ with the shortcomings of inadequate etching bias, etching profiles, premature etch stop, unintentional overetching of contact regions, and etch opening misalignment.

Please replace paragraph 004 with the following re-written paragraph:

004 For example, in prior art processes, a metal filled contact interconnect or via ~~have~~ has been used to make contact from the active contact regions including gate electrode and S/D regions to the first metallization layer through a single

[[I]]interlayer-dielectric (ILD) layer, also referred to as a pre-metal dielectric (PMD) layer. In prior art approaches, The ILD layer is formed overlying the active devices followed by formation of metal filled contacts extending through the ILD layer thickness to electrically connect the active regions to an overlying metallization layer which begins the formation of wiring circuitry formed in multiple overlying metallization levels.

Please replace paragraphs 006 with the following re-written paragraph:

006 These and other shortcomings demonstrate a need in the semiconductor device integrated circuit manufacturing art for improved contact interconnect[[s]] structures and a method for forming the same to form more reliable contact interconnects having smaller width dimensions while avoiding the various shortcomings of the prior art.

Please replace paragraphs 007 with the following re-written paragraph:

007 It is therefore an object of the present invention to provide improved contact interconnect[[s]] structures and a

method for forming the same to form more reliable contact interconnects having smaller width dimensions while avoiding the various shortcomings of the prior art.

Please replace paragraphs 0015 with the following re-written paragraph:

0015 CMOS devices (e.g., FET transistors) 10A, 10B, 10C may form a portion of a logic or memory circuit and may be formed by conventional methods with conventional materials including first conductive active contact regions e.g., 14, for example formed over source/drain regions. The CMOS devices include respective gate structures which include conventional gate dielectric portions e.g., 16 and respective overlying gate electrode portions e.g., 18[[C]]. In addition, the respective gate[[s]] structures include pairs of offset spacers e.g., 20 on either side of the gate structure[[s]] formed of silicon oxide, silicon nitride, silicon oxynitride or combinations thereof. The semiconductor substrate 12 may be formed of silicon, silicon on insulator (SOI), strained silicon, and silicon-germanium (SiGe), or combinations thereof.

Please replace paragraphs 0016 with the following re-written paragraph:

0016 Still referring to Figure 1A, the gate structures including gate dielectric portions may be formed by conventional CVD deposition, lithographic patterning, and plasma and/or wet etching methods known in the art. The gate dielectric may be formed by any process known in the art, e.g., thermal oxidation, nitridation, sputter deposition, or chemical vapor deposition. [[S]]silicon oxide, silicon nitride, silicon oxynitride, high-K (e.g., K > 8) dielectrics including transition metal oxides and rare earth oxides ~~may be used for the gate dielectrics~~.

Please replace paragraphs 0017 with the following re-written paragraph:

0017 The gate electrode portion e.g., 18~~A, 18B, 18C~~ of the gate structure may be formed of polysilicon, polysilicon-germanium, metals, metal silicides, metal nitrides, or conductive metal oxides. Second conductive active contact regions e.g., 19 are optionally formed in the uppermost portion of the gate electrodes along with first conductive contact regions e.g., 14 by conventional CVD or sputtering methods including silicidation to form self-aligned silicides a/s is known in the art. Preferably, the first and second active contact regions include one or a combination of conductive materials ~~such as~~ including

metals, such as Ti, Co, Ni, Pt, W and silicides thereof, e.g., $TiSi_2$, $CoSi_2$, NiSi, PtSi, WSi_2, as well as metal nitrides such as TiN and TaN, or combinations of the foregoing.

Please replace paragraphs 0019 with the following re-written paragraph:

0019 Referring to Figure 1B, according to an important aspect of the invention, a first insulating dielectric (ILD) layer e.g., 22A is blanket deposited by conventional methods, e.g., LPCVD, or PECVD over the process surface, followed by a conventional planarization process such as CMP. Preferably, the first ILD layer 22A is formed of one or [[a]] combinations of PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, SiC, nitrogen doped silicon oxide, silicon nitride (e.g., Si_3N_4), silicon oxynitride (e.g., SiON), low-K (K < 2.9) or high-K (K > 5) dielectrics, and fluorine doped silicon oxide (e.g., FSG). In one embodiment, the first ILD layer 22A is deposited in a two step process to form a first lower contact etch stop layer portion 22AA including one or combinations of, SiC, nitrogen doped silicon oxide, silicon nitride (e.g., Si_3N_4), and silicon oxynitride (e.g., SiON) followed by deposition of and an upper portion including one or combinations of PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, low-K

(K < 2.9) or high-K (K > 5) dielectrics, and fluorine doped silicon oxide (e.g., FSG).

Please replace paragraphs 0023 with the following re-written paragraph:

0023 Referring to Figure 1C, following formation of an inorganic or organic ARC layer 24B one or more resist layers e.g., 26 is deposited and patterned. The resist layer 26 may be a single or multiple layer resist including organic and inorganic materials, for example a lower organic resist layer and an overlying resist including silicon incorporated by a silylation process or including silicon monomers. The resist layer e.g., 26 may have a total thickness of about 0.1 microns to about 1.0 microns, and is preferably sensitive to wavelengths less than about 400 nm. A lithographic patterning process is carried out including radiation exposure and development by appropriate wet or dry development processes, followed by conventional dry etching processes to etch through the first ILD layer 22A to form a first set of contact openings e.g., 28A, 28B, 28C, 28D, and 28E. The contact openings may be formed in the shape of an oval (circular), butt contact, rectangular (e.g., square), or combinations thereof. For example, the contact openings may include a local interconnect opening, e.g., 28C, having the

preferred aspect ratio at a lowermost (bottom) portion of the contact opening.

Please replace paragraphs 0025 with the following re-written paragraph:

0025 Referring to Figure 1E, according to an important and critical aspect of the invention, at least a second insulating dielectric (ILD) layer e.g., 22B is formed over the first ILD layer 22A such that the first and second (or more) dielectric insulating layers is sufficient to meet a required design thickness to meet a required capacitance. For example, the second ILD layer is formed by blanket depositing by conventional methods, e.g., LPCVD, or PECVD, one or more dielectric layers over the first ILD layer 22A followed by a conventional planarization process such as CMP. Preferably, the second ILD layer 22B is ~~preferably~~ formed in the same manner and using the same preferred materials as the first ILD layer 22A. In one embodiment, the second dielectric layer 22B is deposited in a two step process to form a first lower portion, e.g., a contact etch stop layer, 22BB including one or a combination of SiC, nitrogen doped silicon oxide, silicon nitride (e.g., Si_3N_4), and silicon oxynitride (e.g., SiON) and an upper portion 22B including one or a combination of PETEOS, BPTEOS, BTEOS, PTEOS, TEOS, PEOX, low-K

(K < 2.9) or high-K (K > 5) dielectrics, and fluorine doped silicon oxide (e.g., FSG). In the exemplary embodiment preferably one or more of a hardmask layer 24C and an ARC layer 24D are formed over the ILD layer 22B according to the same preferred embodiments outlined[[s]] for hardmask layer 24A and ARC layer 24B.

Please replace paragraphs 0026 with the following re-written paragraph:

0026 Still [[R]]referring to Figure 1[[F]]E, a similar process as outlined for forming the first set of contact interconnects 30A, 30B, 30C, 30D, and 30E is then carried out to form a second set of contact interconnects e.g., 32A, 32B, and 32C extending through the thickness of the second ILD layer 22B to make contact (e.g., including overlying and at least partially encompassing) portions of the first set of contact interconnects. The second set of contact interconnects is formed according to the same preferred embodiments and aspect ratios as the first set of contact interconnects the first ILD layer 22A. The second set of contact interconnects may have the same or different preferred aspect ratio as the second set of contact interconnects, for example having a smaller aspect ratio to ensure adequate interconnect overlap. In addition, longer (horizontal to the

substrate) contact interconnects e.g., 32A may be formed to conductively connect one or more of the first set of contact openings e.g., 30A and 30B. Preferably, the length of the longer contact interconnects, e.g., 32A is between about 0.15 microns and about 500 microns.